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DIGITAL OPTICS FOR NUMERICAL COMPUTING: THE RESIDUE NUMBER SYSTEM FOR NUMERICAL OPTICAL COMPUTING

The BDM Corporation

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The use of Residue Number System (RNS) in performing high accuracy numerical computing with digital optics is investigated. The analysis is focused on the position coded residue representation and the Look Up Table (LUT) approach to arithmetic operations. Two approaches to reducing the total number of LUT entries (the spatial complexity) proposed by Boeing Aerospace Corp. and Westinghouse are studied. Analytical expressions for the spatial complexity, time complexity, and element complexity as a function of the modulus are derived for the two approaches in performing the standard operations of multiplication, addition and for the multiply-accumulate unit. The report thus provides a hardware-independent method of studying the trade-offs between these two major approaches to RNS optical computing. Hardware options for optical implementations of interconnects and nonlinear switching elements are outlined. The intimate relation between the algorithms, architectures and the hardware and their combined impact on the system performance is outlined suggesting directions for future work.

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SUMMARY

The need for high precision numerical computing is central to both scientific and general purpose computation. In achieving this high precision, conventional computers have employed weighted number systems with a fixed radix (base), e.g. the binary number system (base 2). Advantages of such weighted number systems include the ease with which magnitude comparison, sign detection, overflow detection, digital-to-analog conversion, dynamic range extension, and multiplication or division by a power of the base can be performed. However, for arithmetic operations such as addition, subtraction and multiplication, inherent propagation of carries between successive digits precludes truly parallel computation in a weighted number system. Furthermore, this characteristic imposes a fundamental limitation on the speed at which arithmetic computation can be performed.

Approaches to sidestep the speed limitation can generally be classified into two main categories. First, one can "look ahead" and calculate the carries, reducing the carry propagation time at the cost of additional circuitry.

The second approach is to consider alternate number systems for data representation and computation which have unique characteristics with respect to carries. We will follow the latter approach and consider the Residue Number System (RNS) for high-speed, high-accuracy numerical computation.

Another variable when considering numerical computation is the choice of computing media. Optics appears as a good host for RNS-based computation due to the fact that many features of the RNS couple well with optical processing. Natural cyclic phenomena such as polarization and phase of light beams are candidates for residue representation which is also cyclic. Both residue and optics also present the capability to perform parallel carry-free computation. The RNS also exhibits the feature of dividing high-accuracy computation into several independent medium-accuracy "modules." Linear optical systems implementing global interconnects in conjunction with fast simple optical and hybrid nonlinear devices represents another viable approach to performing RNS computation.

As early as 1932, optics and RNS have been united to perform numerical computation. However, only in the past 15 years have the mutual properties been used to gain some computational advantage. The most general form of RNS optical processing is realized by look-up tables (LUTs). Recently two groups, Westinghouse and Boeing Aerospace, have proposed position coded (PCR) LUT - based processing systems which provide a reduction in the complexity associated with LUT processing. The complexity savings result from exploiting key features of remainder arithmetic found in LUT processing.

Under this task, we present an analysis of the optical residue look-up table processors. The initial stage of the study is an investigation of the unique features of RNS arithmetic which become visible when realized in LUT architectures, namely constant cross-diagonal elements of the addition LUT and the zero row and column of the multiplication LUT resulting from multiplication by zero. These features are expressed in terms of cyclic properties of RNS arithmetic and traced to their foundation in Group Theory. Addition (modulo m) is inherently a group operation, and multiplication (modulo m) can be transformed into a group operation (modulo m-1), both of which possess the advantages of group operation LUT processing.

These insights are subsequently used to study the particular Westinghouse and Boeing approaches to RNS LUT processing. Considering the RNS modular representation as factoring the system dynamic range, the Westinghouse group has proposed a "second-level factorization" of the moduli, further reducing the system complexity. The above mentioned RNS multiplication properties allow factoring (m-1) (for each modulus m) into p factors $(k_1,...,k_p)$. Processing is performed in p independent $(k_i \times k_i)$ LUTs, leading to a significant reduction in the total number of LUT entries. However, addition proves to be more complex in the factored domain. The Boeing LUT processor is based on the cross-diagonal symmetry present in group operation tables. For LUT processing, one only needs to locate the appropriate cross-diagonal of the table for the calculation of the output, effectively reducing the number of table locations. As mentioned, the addition LUT possesses this symmetry and the multiplication LUT can be transformed into a symmetric group table.

With the proper RNS and LUT arithmetic processing background, the next step is performance analysis. We present a comparative study of the currently-proposed optical LUT processors with respect to traditional LUT processors from an architectural standpoint. The approach is to specify the LUT processors in terms of fundamental arithmetic processing units (APUs), namely multipliers, adders, and multiplier-accumulators (MAUs). The idea is that carefully specifying the APUs, and maintaining that input and output data formats must be compatible, will provide common ground which equalizes the processors and reveals all costs. In an effort to decouple the architectures from hardware specifics, "computational components" are chosen as the fundamental blocks from which the APU architectures will be constructed. These components include basic LUTs, transforms, encoders, decoders, and specialized hardware such as zero-detectors. Along with the APUs, we propose a set of performance criteria on which the architectures are to be evaluated. In an effort to span the range of performance issues and their trade-offs, four high-level criterion are chosen. They are:

(1) temporal complexity - the number of sequential stages required to perform a desired operation,

(2) spatial complexity - the number of active decision-making elements in the system,

(3) interconnect complexity - measured as a function of the average "fan-out" per input channel and "fan-in" to each output channel. The interconnects can also be classified according to uniformity from channel to channel as "shift variant" or "shift invariant,"

(4) element complexity - the average number of resolvable levels required of the active elements, i.e. the element dynamic range.

Notice that the performance criteria can all be related to specific cost issues at the hardware level.

The performance analysis proceeds as follows. The fundamental components are specified in block form and analyzed on the basis of our listed criteria. The component complexities are listed in a table for easy access and comparison. Multiplier, adder and MAU block diagrams are then built from these components for each specific approach. Evaluation at the APU level consists of simply adding the complexities of each of the components. The results of APU complexity for each approach, Westinghouse, Boeing and direct, are compiled in a table. However, spatial complexity shows a strong dependence upon moduli, which can best be seen in graphical format, and therefore, is plotted. Conclusions regarding the relative performance of the LUT architectures as a function of modulus, as well as general conclusions, can be readily extracted from the resulting tables and graphs.

The next dimension in the LUT performance analysis is a discussion of hardware issues. Overall system performance parameters, such as throughput, power consumption, connectivity, and stability are determined by combining the architectural characteristics with hardware characteristics. From the previous analysis, required hardware can be divided into two categories, interconnects and active switching elements. The architectural analysis provides the mapping from algorithms to devices, that is, the hardware selection is guided by the architecture for each particular approach to LUT processing. In this section, we identify the requirements for interconnects and switching elements as dictated by the processing components. Next, we list the various optical technologies capable of performing the required connection or switch, along with the respective advantages and disadvantages. It becomes apparent that there is a level of interaction and associated trade-offs between architectures and hardware. In this light, we see that the architectures help specify which technology is most amenable to that type of LUT processing. Alternately, one might also conclude that no device technology meets the requirements of a particular architecture.

In summary, we adopt a systematic and comprehensive approach to investigating optical RNS processing. We identify the algorithms and architectures of three approaches to LUT processing on the common ground of arithmetic processing units. Performance criteria are chosen such that cost trade-offs are made explicit and not postponed. The architectures are then mapped onto devices and technologies suited to the particular approach. It is felt that only in this domain can one fully assess a reduction in complexity of one approach over another. Such a systematic approach has helped us in identifying the complexities of the two leading approaches (Boeing and Westinghouse) for computationally useful operations and furthermore helped us locate the origins. This understanding cannot be obtained by a totally integrated performance analysis that gives a parts count, throughput and power consumption estimation for a specific hardware implementation of a specific architecture which is based upon a specific algorithm.

The report will proceed as follows. The first section is a tutorial on the basics of residue arithmetic, including various advantages and disadvantages of the number system. The next section provides some background by tracing the history of RNS-based optical processing. Following the introductory material, we will focus our sights down to optical LUT processing, and will investigate key features of the RNS which make the more recent approaches attractive. The fourth section presents the detailed architectural performance analysis of optical RNS LUT processing based on fundamental performance criteria and fundamental computational units. The next section presents the results of the performance analysis, along with conclusions based upon the results. In the last section, we will map the architectural results onto hardware considerations, rounding out the analysis. The report concludes with a comprehensive general reference section.

THE RESIDUE NUMBER SYSTEM FOR NUMERICAL OPTICAL COMPUTING

OUTLINE

I. INTRODUCTION TO RNS: A TUTORIAL

II. RNS IN OPTICAL PROCESSING

III. OPTICAL RNS LOOK-UP TABLE PROCESSING

IV. PERFORMANCE ANALYSIS OF LOOK-UP TABLE PROCESSING

V. RESULTS

VI. HARDWARE CONSIDERATIONS

WHY RESIDUE?

* IN TRADITIONAL WEIGHTED NUMBER SYSTEMS (BINARY, DECIMAL, ..), INHERENT PROPAGATION OF CARRIES PRECLUDES TRULY PARALLEL COMPUTATION.

=> THIS POSES A FUNDAMENTAL LIMITATION ON THE SPEED AT WHICH ARITHMETIC OPERATIONS CAN BE PERFORMED.

* TWO APPROACHES TO CIRCUMVENT THE LIMITATION:

I. ADDITIONAL CIRCUITRY TO LOOK-AHEAD

II. ALTERNATE NUMBER SYSTEMS WITH SPECIAL CARRY CHARACTERISTICS

INTRODUCTION TO THE RESIDUE NUMBER SYSTEM:

A TUTORIAL

THE RESIDUE NUMBER SYSTEM

* SELECT N PAIRWISE RELATIVELY PRIME INTEGER MODULI

  $m_1, m_2, \ldots, m_N$ AS SYSTEM BASE

* INTEGER X IS REPRESENTED AS AN N-TUPLE OF RESIDUES

  $X \Rightarrow (R_1, R_2, \ldots, R_N)$

  where R_i = the RESIDUE of X modulo m_i

  $= |X|_{m_i}$

  and $0 \le R_i \le m_i - 1$ for each R_i

* THE REPRESENTATION FOR X IS UNIQUE IN THE DOMAIN

  $0 \le X \le M-1$, where $M = m_1 * m_2 * \ldots * m_N$

e.g. TO PERFORM A 16-bit MULTIPLY REQUIRES 32-bit DYNAMIC RANGE -> m_i = 5,7,9,11,13,16,17,19,23

* EXAMPLE:

  BASE MODULI: m_i = 2,3,5

  INTEGERS: $X_1 = 7$ $X_2 = 4$

  REPRESENTATION: $X_1 \Rightarrow (1,1,2)$ $X_2 \Rightarrow (0,1,4)$

  ADDITIVE INVERSE $-X_i = |m_i - R_i|_{m_i}$

  $-X_1 \Rightarrow (1,2,3)$ $-X_2 \Rightarrow (0,2,1)$

  DYNAMIC RANGE: $M = 2*3*5 = 30$

THE RESIDUE NUMBER SYSTEM

* DECODING THE RESIDUE REPRESENTATION

THE CHINESE REMAINDER THEOREM:

- PERFORMS RESIDUE TO ANALOG CONVERSION
- GIVEN THE RESIDUE REPRESENTATION $(R_1, R_2, \ldots, R_N)$ THE CRT DETERMINES $|X|_M$

PROBLEM: REQUIRES AN ANALOG SYSTEM WITH FULL DYNAMIC RANGE (M not m_i)

$$|X|_M = \left| \sum_{j=1}^{N} \hat{m}_j \left| \frac{r_j}{\hat{m}_j} \right|_{m_j} \right|_M$$

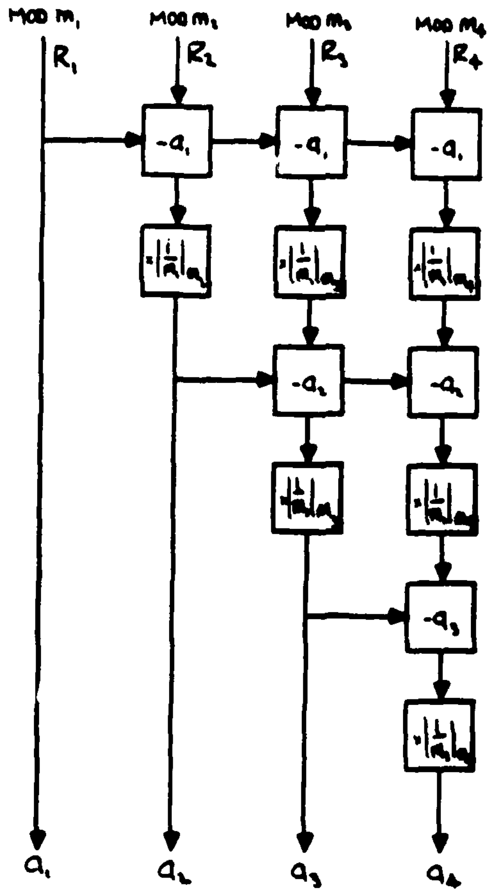
WHERE $\hat{m}_j = M/m_j$

THE RESIDUE NUMBER SYSTEM

MIXED-RADIX CONVERSION:

CONVERSION FROM THE RESIDUE REPRESENTATION TO A WEIGHTED NUMBER SYSTEM

- REQUIRES OPERATIONS MODULO m_i ONLY
- REQUIRES N-1 SEQUENTIAL STAGES



$$X = a_1 + a_2 * m_1 + a_3 * m_1 * m_2 + a_4 * m_1 * m_2 * m_3$$

RESIDUE ARITHMETIC

* ADDITION: PERFORM MODULO m_i ADDITION OF CORRESPONDING RESIDUES FOR EACH MODULUS

EXAMPLE: $X_1 + X_2$

$$\begin{array}{r}
7 \Rightarrow (1,1,2) \\
\underline{+\ 4 \Rightarrow (0,1,4)} \\
(1,2,1) \Leftarrow 11
\end{array}$$

* SUBTRACTION: FIND THE ADDITIVE INVERSE OF THE SUBTRAHEND AND THEN PERFORM ADDITION

EXAMPLE: $X_1 - X_2 = X_1 + (-X_2)$

$$\begin{array}{r}
7 \Rightarrow (1,1,2) \\
\underline{+(-4) \Rightarrow (0,2,1)} \\
(1,0,3) \Leftarrow 3
\end{array}$$

* MULTIPLICATION: MULTIPLY CORRESPONDING RESIDUES AND FIND THE RESIDUE OF THE PRODUCT MODULO m_i

EXAMPLE: $X_1 * X_2$

$$\begin{array}{r}
7 \Rightarrow (1,1,2) \\
\underline{\times\ 4 \Rightarrow (0,1,4)} \\
(0,1,3) \Leftarrow 28
\end{array}$$

* DIVISION: GENERALLY NOT POSSIBLE

FEATURES OF THE RESIDUE NUMBER SYSTEM

* ABILITY TO DECOMPOSE A CALCULATION INTO SUBCALCULATIONS OF REDUCED COMPUTATIONAL COMPLEXITY

  => SUBCALCULATION ACCURACY REQUIREMENT COMMENSURATE WITH PARTICULAR MODULUS

* SUBCALCULATIONS ARE INHERENTLY INDEPENDENT AND ARE PERFORMED IN SEPARATE UNITS

  => PARALLEL CARRY-FREE ADDITION, SUBTRACTION, AND MULTIPLICATION

* LARGE DYNAMIC RANGE
  - EXPANDABLE BY INCLUSION OF ADDITIONAL MODULI

* RNS IS A CYCLIC NUMBER SYSTEM:
  - INTERMEDIATE COMPUTATION RESULTS CAN OVERFLOW SYSTEM DYNAMIC RANGE WITHOUT ERROR IN RESULT

  EXAMPLE: (7*5)-9 = 35-9 = 26

  (1,1,2) * (1,2,0) = (1,2,0)

  (1,2,0) - (1,0,4) = (1,2,0) + (1,0,1) = (0,2,1)

PROBLEMS WITH THE RESIDUE NUMBER SYSTEM

SOME OPERATIONS IN THE RNS ARE SLOWED BY THE NECESSITY TO CONVERT TO A WEIGHTED REPRESENTATION WHICH IS *INHERENTLY-SEQUENTIAL*

* RELATIVE MAGNITUDE COMPARISON
* ALGEBRAIC SIGN DETECTION
* DYNAMIC RANGE OVERFLOW DETECTION
* DIVISION

OPTICS AND RNS:

A HISTORICAL PERSPECTIVE

MOTIVATION

MANY RNS FEATURES COUPLE WELL WITH OPTICS

* REDUCED DYNAMIC RANGE REQUIREMENTS OF PROCESSING UNITS

  >2 , but $<<1000$

* PARALLEL, CARRY-FREE COMPUTATION

* CYCLIC NATURE OF RESIDUE REPRESENTATION COUPLES WITH NATURAL CYCLIC PHENOMENA FOUND IN LIGHT BEAMS

  (polarization, phase, diffraction)

* CONVENIENT FOR LOOK-UP TABLE PROCESSING
  - FAN-OUT / FAN-IN CAPABILITIES
  - 3-D INTERCONNECTS

HISTORICAL PERSPECTIVE

ANCIENT OPTICAL SYSTEM

* PHOTO-ELECTRIC NUMBER SIEVE, D.H. LEMER, 1932
  - FOR HIGH DYNAMIC RANGE COMPUTING BEFORE EMERGENCE OF THE ELECTRONIC COMPUTER
  - EMPLOYS LIGHT BEAM AND PHOTO-CELLS TO SENSE OPENINGS AND CLOSINGS OF MECHANICAL SIEVE
  - 30 GEARS, ONE FOR EACH PRIME TO 113
  - USED TO FACTOR NUMBERS, SUCH AS THE MERSENNE NUMBER
  - SIFTED 20,000,000 NUMBERS PER HOUR

ANALOG REPRESENTATION

* A. HUANG, 1975
  - FIRST TO SUGGEST COUPLING PROPERTIES OF RNS WITH OPTICAL NUMERIC COMPUTING

* S. COLLINS, 1977
  - PROCESSOR BASED ON RESIDUE REPRESENTATION BY POLARIZATION AND PHASE STATES OF OPTICAL BEAM

PROBLEM: REQUIRED RESOLUTION OF OPTICAL COMPONENTS

for $m=37$ => resolution$=2\pi/37$ radians

HISTORICAL PERSPECTIVE

BINARY-CODED RESIDUE (BCR) BASED SYSTEMS

- RESIDUES ARE REPRESENTED IN THEIR BINARY FORM
- REQUIRES $\lceil \log_2(m_i) \rceil$ BITS PER MODULUS

* CONTENT-ADDRESSABLE MEMORY, C. GUEST AND T. GAYLORD, 1980

  - BASED ON TRUTH-TABLE LOOK-UP PROCESSING
  - CAM STORES THE CANONICAL SUM-OF-PRODUCTS REPRESENTATION OF EACH OUTPUT BIT
  - EMPLOY LOGICAL MINIMIZATION TO REDUCE THE NUMBER OF REFERENCE PATTERNS THE CAM MUST STORE

HISTORICAL PERSPECTIVE

POSITION-CODED RESIDUE (PCR) BASED SYSTEMS

- RESIDUES ARE REPRESENTED BY THE SPATIAL POSITION OF LIGHT

* THE OPTICAL WHEEL, F. HORRIGAN AND W. STONER, 1979
  - PROMPTED BY CYCLIC NATURE OF KALEIDOSCOPE OPTICS
  - "OPTICAL PISTON" DEMONSTRATED MAPPING INPUT POSITIONS INTO CYCLIC OUTPUT POSITIONS

* CORRELATION APPROACH, D. PSALTIS AND D. CASASENT, 1979
  - LINEAR SYSTEM, CORRELATION-BASED FORMULATION OF RESIDUE ARITHMETIC
  - EMPLOY POSITION CODING, CARRIER MODULATION AND APERTURE CONTROL TO ACHIEVE RNS OPERATIONS

* MAPPING APPROACH, A. HUANG, ET AL. 1979
  - IMPLEMENT RESIDUE ARITHMETIC OPERATIONS WITH MAPS WHICH PERFORM PERMUTATION OF THE INPUT DATA
  - MAP BANKS ARE USED TO REALIZE CHANGEABLE MAPS
  - EMPLOYS CHANGEABLE MAPS FOR CYCLIC PERMUTATIONS

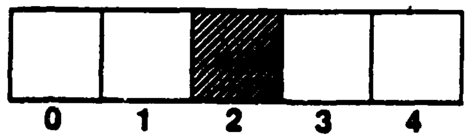
OPTICS AND RNS:

LOOK-UP TABLE PROCESSING

RECENT APPROACHES TO OPTICAL NUMERICAL COMPUTING USING RESIDUE ARITHMETIC

RNS LOOK-UP TABLE PROCESSING
THE BASICS

* PCR ENCODING IN "ONE OUT OF m" CONFIGURATION



* TABLE LOOK-UP PROCESSING:

MODULO m LUTs REQUIRE m^2 TABLE ENTRIES

EXAMPLES: MODULO 5 ADDITION AND MULTIPLICATION OF 2 AND 3

+	0	1	2	3	4
0	0	1	2	3	4
1	1	2	3	4	0
2	2	3	4	0	1
3	3	4	0	1	2
4	4	0	1	2	3

ANSWER = 0

x	0	1	2	3	4
0	0	0	0	0	0
1	0	1	2	3	4
2	0	2	4	1	3
3	0	3	1	4	2
4	0	4	3	2	1

ANSWER = 1

PROCESSING IS REALIZED IN MANY WAYS:

- INPUT POSITIONS PROVIDE ROW AND COLUMN ADDRESS FOR LUT
- FOR A GIVEN INPUT WORD, SECOND INPUT SELECTS MAP WHICH CORRECTLY PERMUTES INPUTS FOR GIVEN OPERATION

RNS LOOK-UP TABLE PROCESSING

KEY FEATURES

ADDITION MODULO 5

+	0	1	2	3	4
0	0	1	2	3	4
1	1	2	3	4	0
2	2	3	4	0	1
3	3	4	0	1	2
4	4	0	1	2	3

MULTIPLICATION MODULO 5

×	0	1	2	3	4
0	0	0	0	0	0
1	0	1	2	3	4
2	0	2	4	1	3
3	0	3	1	4	2
4	0	4	3	2	1

* ADDITION TABLE
  - NOTE THAT ROW AND COLUMN ENTRIES SPAN THE RESIDUE SET IN A CYCLIC FASHION
  - NOTE THE CROSS-DIAGONAL SYMMETRY PRESENT IN THE TABLE
  - NOTE THE CYCLIC PERMUTATION OF THOSE CROSS-DIAGONALS

* MULTIPLICATION TABLE
  - NOTE ZERO ROW AND COLUMN RESULTANT FROM MULTIPLICATION BY ZERO
  - EXCLUSION OF ZERO ROW AND COLUMN RESULTS IN ROWS AND COLUMNS THAT SPAN A REDUCED RESIDUE SET

PROPERTIES OF RESIDUE ARITHMETIC

ADDITIONAL PROPERTIES OF THE RNS CAN BE EXPRESSED IN TERMS OF *GROUP THEORY*

* THE SET OF INTEGERS 0,1,2,...,m-1 (residues of MODULUS m) FORM A *GROUP* UNDER ADDITION MODULO m

* THE SET OF INTEGERS 1,2,3,...,m-1 (reduced residue set) FORM A *GROUP* UNDER MULTIPLICATION MODULO m

* BOTH OF THESE GROUPS ARE *CYCLIC* UNDER THE GIVEN OPERATION
  - A CYCLIC GROUP MUST HAVE AT LEAST ONE *GENERATOR*

* THE GENERATOR IS AN ELEMENT OF THE GROUP
  - SUCCESSIVE GROUP OPERATIONS UPON THE GENERATOR DETERMINES THE CYCLIC SEQUENCE

    -> "1" IS ALWAYS A GENERATOR FOR ADDITION MODULO m

    -> GENERATORS FOR MULTIPLICATION MODULO m DEPEND UPON m

THE OPERATION TABLE FOR CYCLIC GROUPS

@	F^0	F^1	F^2	.	.	.	F^{m-1}
F^0	F^0	F^1	F^2	.	.	.	F^{m-1}
F^1	F^1	F^2	F^3	.	.	.	F^0
F^2	F^2	F^3	F^4	.	.	.	F^1
.	.	.	.	.			.
.	.	.	.		.		.
.	.	.	.			.	.
F^{m-1}	F^{m-1}	F^0	F^1	.	.	.	F^{m-2}

@ = GROUP OPERATION

F^0 = IDENTITY ELEMENT

F^1 = GENERATOR

$F^i = F^1 @ F^1 @ F^1 @ \ldots @ F^1$ (i TIMES)

$F^m = F^0$

EXAMPLE: MODULO 5 GROUP OPERATIONS

GROUP OPERATION OF ADDITION:

- THE RESIDUES (0,1,2,3,4) FORM A CYCLIC GROUP UNDER ADDITION MODULO 5
- $F^1=1$ IS ALWAYS A GROUP GENERATOR
- THE OPERATION TABLE IS IDENTICAL TO THE LOOK-UP TABLE

GROUP OPERATION OF MULTIPLICATION:

- THE INTEGERS (1,2,3,4) FORM A CYCLIC GROUP UNDER MULTIPLICATION MODULO 5
- $F^1=3$ IS A GROUP GENERATOR

  $3^0=1 \quad 3^1=3 \quad 3^2=4 \quad 3^3=2 \quad (3^4=3^0=1)$
- CYCLIC ORDERING IS THEN (1,3,4,2)
- OPERATION TABLE IS REALIZED AS REDUCED $(m-1 \times m-1)$ TRUTH TABLE WITH ROWS AND COLUMNS RESEQUENCED

x	1	3	4	2
1	1	3	4	2
3	3	4	2	1
4	4	2	1	3
2	2	1	3	4

* NOTICE THAT THE LUT NOW EXHIBITS ALL THE CYCLIC PROPERTIES

LOGARITHMIC TRANSFORMATION FOR MULTIPLICATION

* SINCE THE MULTIPLICATION TABLE CAN BE TRANSFORMED INTO A GROUP OPERATION TABLE, THE CHOICE OF GROUP OPERATION BECOMES ARBITRARY

* THUS, THE RESEQUENCED MULTIPLICATION LOOK-UP TABLE CAN BE REPLACED WITH AN ADDITION TABLE

  -> NEED ONLY TO KEEP TRACK OF THE PERMUTATION MAPPING

LOGARITHMIC TRANSFORMATION

- THE GENERATOR PROVIDES THE KEY TO THE TRANSFORMATION
- TAKING THE GENERATOR-BASED LOG OF THE INTEGER POWERS WHICH GENERATE THE GROUP PROVIDES A TRANSFORMATION WHICH MAPS THE $1,2,...,m-1$ CYCLIC GROUP UNDER MULTIPLICATION MODULO m ONTO THE $0,1,...,m-2$ CYCLIC GROUP UNDER ADDITION MODULO $m-1$

  * MULTIPLICATION MODULO m ==> ADDITION MODULO $m-1$

SUMMARY: MODULAR ADDITION IS A CYCLIC GROUP OPERATION AND MODULAR MULTIPLICATION CAN BE TRANSFORMED INTO A CYCLIC GROUP OPERATION

RNS LOOK-UP TABLE PROCESSING
TWO RECENT APPROACHES

* MOST LUT ARCHITECTURES PROPOSED REQUIRE ACTIVE ELEMENTS FOR EACH TABLE ENTRY

  => SPATIAL COMPLEXITY = m^2

* THIS IMPOSES LIMITATIONS ON THE RANGE OF ACCEPTABLE MODULI

* RECENT EFFORTS HAVE CENTERED ON EXPLOITING THE CYCLIC GROUP PROPERTIES OF RESIDUE ARITHMETIC TO REDUCE NUMBER OF LUT ENTRIES

  FACTORED LOOK-UP TABLES

  WESTINGHOUSE: GOUTZOULIS, MALARKEY, DAVIES, BRADLEY, and BEAUDET

  CROSS-DIAGONAL-SYMMETRIC LOOK-UP TABLES

  BOEING AEROSPACE: C. CAPPS, R. FALK AND T. HOUK

FACTORED LOOK-UP TABLES

* THE RNS REPRESENTATION CAN BE VIEWED AS "FACTORING" AT THE FIRST LEVEL, PROPERTIES OF MULTIPLICATION MODULO m ALLOW FACTORING AT A SECOND LEVEL

ALGORITHM: "DIRECT" METHOD

- FOR PRIME m, m-1 IS EVEN AND CAN BE FACTORED INTO PAIRWISE RELATIVE PRIMES

  $$m-1 = k_1 * k_2 * \ldots * k_p$$

- GENERATORS SPECIFY THE ELEMENTS OF p SUBGROUPS
  - iTH SUBGROUP HAS DIMENSION k_i
  - SUBGROUPS ARE CYCLIC (THEOREM)
- EACH RESIDUE DIGIT, FOR A PARTICULAR MODULUS m_j, IS NOW REPRESENTED AS A p-TUPLE OF SUB-RESIDUES

  $$R_j \Rightarrow (R_{j1}, R_{j2}, \ldots, R_{jp})$$

- PROCESSING IS PERFORMED IN p SEPARATE LUTs OF DIMENSION $k_i \times k_i$

* ALSO PERFORM FACTORING WITH "LOGARITHMIC" METHOD
* FACTORED ADDITION IS MORE COMPLEX FOR EITHER METHOD

EXAMPLE: FACTORED LUT PROCESSING

DIRECT APPROACH

MODULUS = 7

RESIDUES: 0,1,2,3,4,5,6

REDUCED SET: 1,2,3,4,5,6

FACTOR: $6=2*3$

GENERATORS: $2^0=1$ $2^1=2$ $2^2=4$ $2^3=2^0=1$

$6^0=1$ $6^1=6$ $6^2=6^0=1$

SUBGROUPS: 2 ELEMENT => (1,6)

3 ELEMENT => (1,2,4)

ENCODING: 1=(1,1) 2=(1,4) 3=(6,2) 4=(1,2) 5=(6,4) 6=(6,1)

LUTs:

x	1	6
1	1	6
6	6	1

x	1	2	4
1	1	2	4
2	2	4	1
4	4	1	2

EX: 3*6 MODULO 7 => (6,2)*(6,1) = (1,2) => 4

NOTE: COULD HAVE PERFORMED THE MULTIPLICATION IN ADDITION TABLES USING THE LOGARITHMIC TRANSFORMATION

CROSS-DIAGONAL-SYMMETRIC LUTs

* EXPLOIT THE CROSS-DIAGONAL SYMMETRY PRESENT IN GROUP TABLES
* A TABLE OPERATION NEED ONLY FIND THE CORRECT CROSS-DIAGONAL

+	0	1	2	3	4
0	0	1	2	3	4
1	1	2	3	4	0
2	2	3	4	0	1
3	3	4	0	1	2
4	4	0	1	2	3

* NOTE CORRESPONDENCE BETWEEN PCR INPUT SOURCE SPACING AND CROSS-DIAGONAL OF TABLE

ALGORITHM:

* ONLY PERFORM OPERATIONS ON CYCLIC TABLES
  - ADDITION MODULO m IS CYCLIC
  - MULTIPLICATION MODULO m CAN BE TRANSFORMED INTO ADDITON MODULO m-1
* ARRANGE INPUTS IN LINEAR ARRAY
* CALCULATE EFFECTIVE DISTANCE BATWEEN INPUTS

=> SPATIAL COMPLEXITY IS REDUCED TO LINEAR DIMENSION

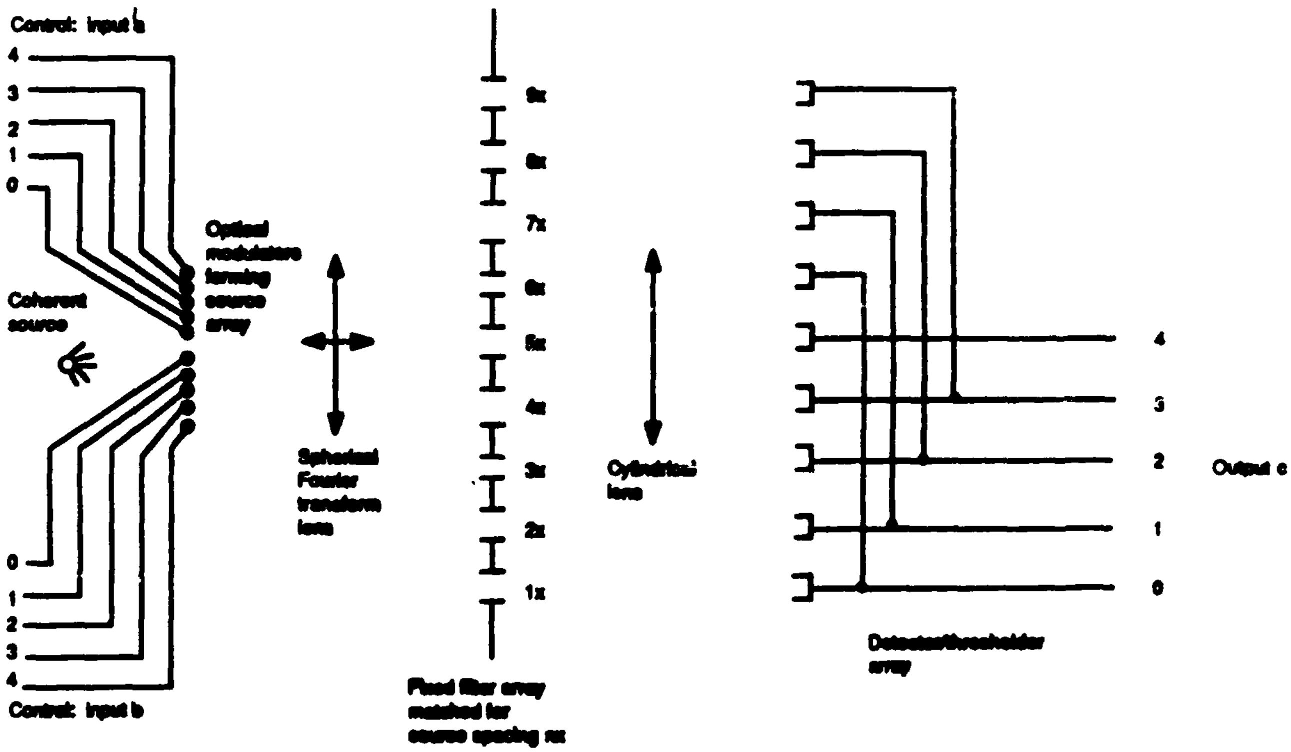


Figure 6. Conceptual Diagram for Parallel Modulo 5 Adder

FROM: CAPPS, FALK, HOUK, "OPTICAL ARITHMETIC/LOGIC UNIT BASED ON SYMBOLIC SUBSTITUTION," TO BE PUBLISHED IN APPLIED OPTICS.

OPTICAL RNS LUT PROCESSING:

PERFORMANCE ANALYSIS

APPROACH

* TO ANALYZE CURRENT LOOK-UP TABLE ARCHITECTURES (WITH RESPECT TO TRADITIONAL LUT ARCHITECTURES) AS ARITHMETIC PROCESSING UNITS.

- BUILD PROCESSING UNITS FROM FUNDAMENTAL COMPUTATIONAL COMPONENTS
- COMPATIBLE INPUT AND OUTPUT DATA FORMATS

=> SPECIFY PERFORMANCE CRITERIA

=> SPECIFY AND ANALYZE COMPUTATIONAL COMPONENTS

=> SPECIFY AND ANALYZE FUNDAMENTAL COMPUTATIONAL UNIT

=> EVALUATE DIFFERENT ALGORITHMS/ARCHITECTURES

PERFORMANCE CRITERIA

* TEMPORAL COMPLEXITY (C_T):

  NUMBER OF SEQUENTIAL STAGES

* SPATIAL COMPLEXITY (C_S):

  NUMBER OF DECISION MAKING ELEMENTS

* INTERCONNECT COMPLEXITY (C_I)

  - AVERAGE FAN-IN (C_{FI}) AND FAN-OUT (C_{FO}) PER CHANNEL
  - "SHIFT VARIANT" OR "SHIFT INVARIANT"

* ELEMENT COMPLEXITY (C_E)

  AVERAGE NUMBER OF RESOLVABLE LEVELS

PROCESSING COMPONENTS:
DEFINITION AND EVALUATION

TRANSFORMATION STAGE

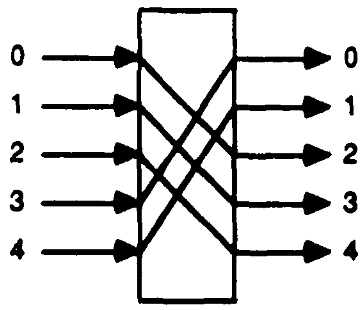
FOR LOGARTIHMIC TRANSFORMATIONS OR ANY FIXED PERMUTATION

$C_T=0$

$C_{[illegible]}=0$

$C_I=1-1$ SHIFT VAR.

$C_{[illegible]}=0$



"+2 MODULO5"

INPUT ENCODER

FOR ENCODING INPUTS INTO FACTORED REPRESENTATION

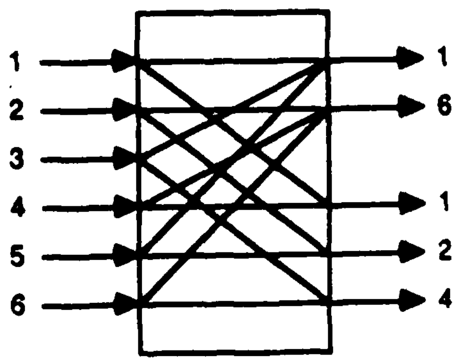
$C_T=0$

$C_{[illegible]}=0$

$C_{PI}=(m-1)/k_1$

$C_{PO}=p$

$C_{[illegible]} \sim C_{PI}$



FACTOR ENCODING

PROCESSING COMPONENTS:

DEFINITION AND EVALUATION

OUTPUT DECODER

DECODING FACTORED OUTPUTS INTO POSITION CODE

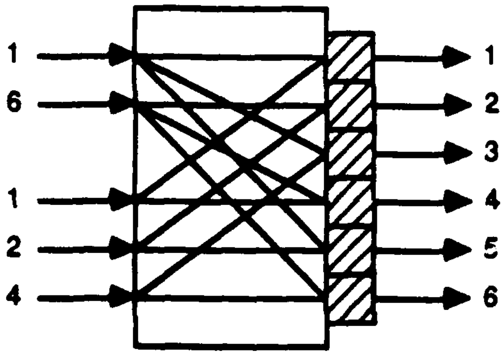
$C_T=1$

$C_S=(m-1)$ number of output lines

$C_{FI}=p$

$C_{FO}=(m-1)/k_1$

$C_E=p:1$



FACTOR DECODING

ZERO DETECTOR

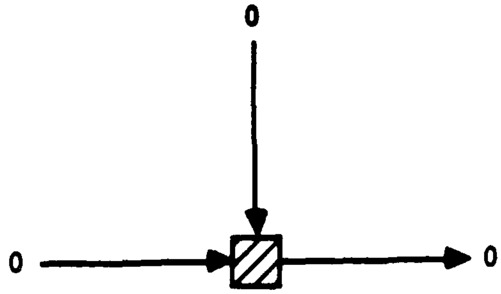
REMOVING ZERO INPUT FOR MULTIPLICATION

$C_T=1$

$C_S=1$

$C_{FI}=2$

$C_E=1:0$



ZERO DETECTOR

PROCESSING COMPONENTS:

DIRECT m^2 LOOK-UP TABLE

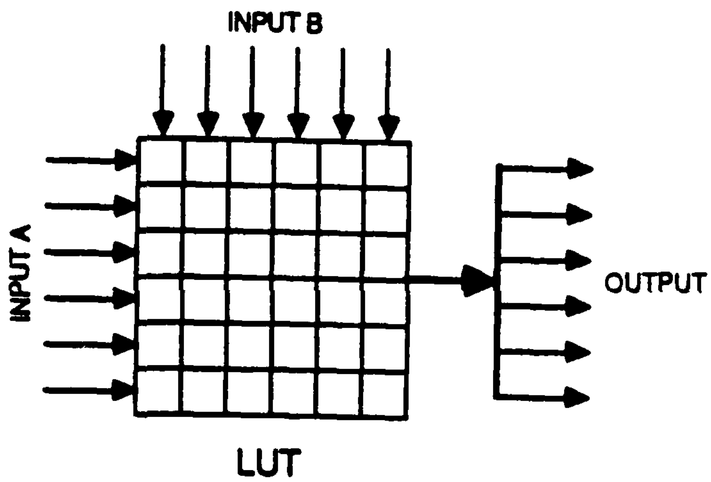
ADDITION AND MULTIPLICATION TABLE ARCHITECTURES ARE IDENTICAL

DESCRIPTION:

2 m-POSITION INPUTS

m-POSITION OUTPUT

m^2 LUT ENTRIES



EVALUATION:

$C_T=1$

$C_S=m^2$

$C_{PO}=m$ SHIFT INVARIANT

$C_{PI}=m$ SHIFT VARIANT

$C_C=2:1$

PROCESSING COMPONENTS:

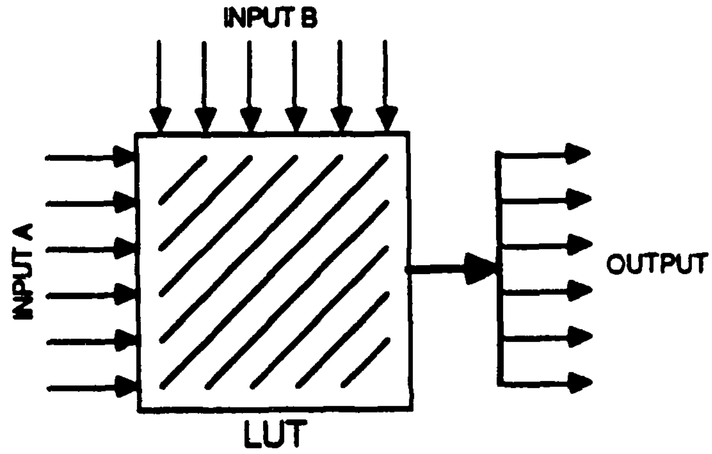
BOEING ADDITION LOOK-UP TABLE

DESCRIPTION:

2 m-POSITION INPUTS

m-POSITION OUTPUT

2m-1 LUT ENTRIES



EVALUATION:

$C_T = 1$

$C_S = 2m-1$

C_{PO} => architecture dependent

C_{PI} => architecture dependent

C_C => architecture dependent

PROCESSING COMPONENTS:

BOEING MULTIPLICATION LOOK-UP TABLE

DESCRIPTION:

INPUT ZERO DETECTION

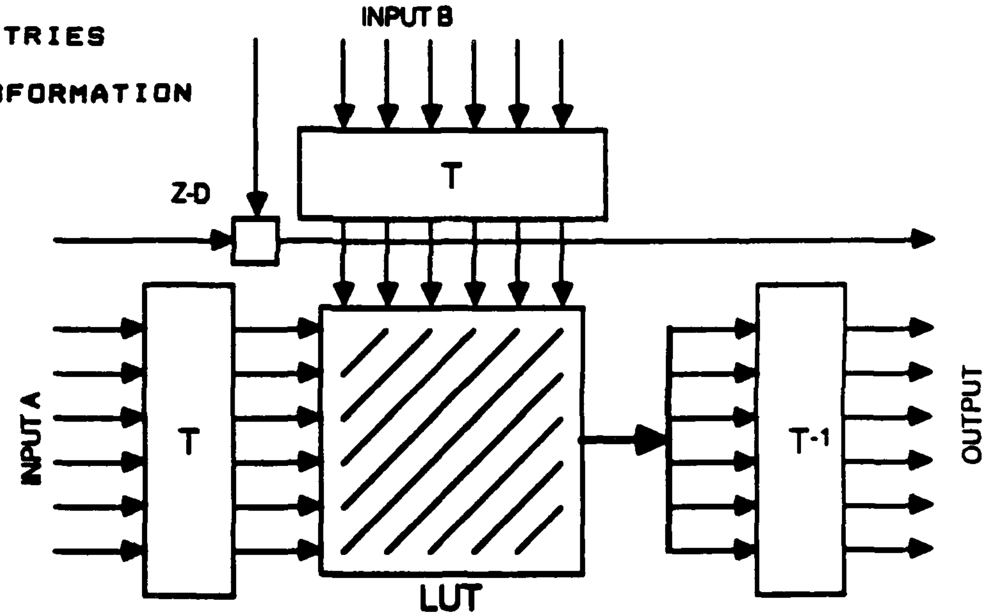
INPUT TRANSFORMATION

2 (m-1) POSITION INPUTS

(m-1) POSITION OUTPUT

2m-3 LUT ENTRIES

OUTPUT TRANSFORMATION



EVALUATION:

$C_T=1$

$C_S=2m-2$

$C_I=>$ C_I transformation

$C_{PO}=>$ architecture dependent

$C_{PI}=>$ architecture dependent

$C_E=>$ architecture dependent

PROCESSING COMPONENTS:

WESTINGHOUSE FACTORED MULTIPLICATION LOOK-UP TABLE

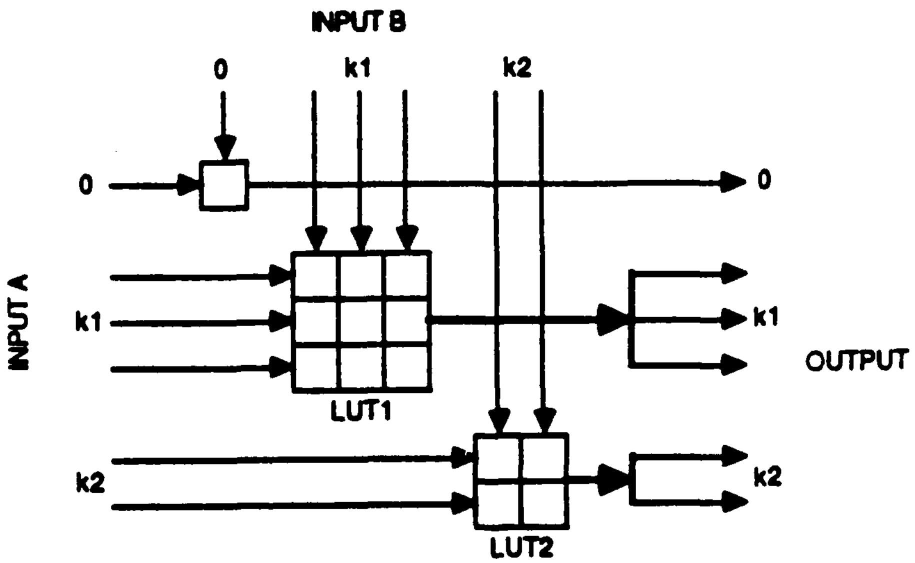
DESCRIPTION:

INPUT ZERO DETECTION

2 k_i POSITION INPUTS, $i=1$ TO p

k_i POSITION OUTPUT

k_i^2 LUT ENTRIES



EVALUATION:

$C_T=1$

$C_S=\sum k_i^2+1$

$C_{PO}=k_i$ SHIFT INV

$C_{PI}=k_i$ SHIFT VAR

$C_R=2:1$

PROCESSING COMPONENTS:

WESTINGHOUSE FACTORED ADDITION LUT

DESCRIPTION:

INPUT ZERO DETECTION AND PASS-THRU

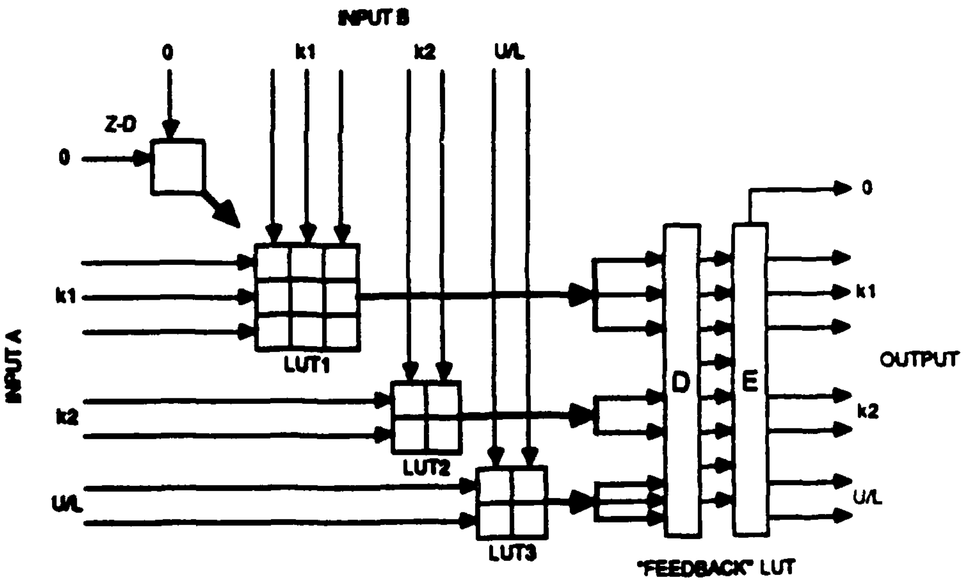
EXTRA INPUT 2-BIT "L"or"U" WORD

$2\ k_i\ (i=1\ \text{to}\ p) + 4$ POSITION INPUTS

$k_i + 2$ POSITION OUTPUT

$k_i^2 + 4$ LUT ENTRIES

"FEEDBACK LUT" RECODES ADDITION OUTPUTS



EVALUATION:

$C_T = 2$

$C_M = \sum k_i^2 + 2\sum k_i + 3m + 1$

$C_{PO} = k_i$ SHIFT INV & decoder & encoder

$C_{PI} = k_i$ SHIFT VAR & decoder & encoder

$C_C = 2:1$ & $p+1:1$

NOTES ON FACTORED ADDITION LUTs

Westinghouse has proposed two main approaches to factored addition: "direct" and "logarithmic." The approaches differ greatly in both algorithm and architecture. In this analysis, we focus on the "direct" method.

First, recall that the motivation for LUT factoring was based on multiplication by zero. The key property is that a zero result can only be produced if either input (or both inputs) is (are) zero, and hence, simple zero-detection removes zero from the input and the output. However, removing zero from the input for modular addition is a different case. Zero can result from additions where neither addend is zero (i.e. 5+2 modulo 7 = 0). Therefore, the LUTs for addition must be capable of identifying m separate output channels, but the factored LUTs can only produce m-1 outputs. Additional information must be carried through the system to produce the extra output.

In terms of processing components, there are three additional units required to perform factored addition over factored multiplication. Their description and related complexities are discussed here.

(1) Zero-detection with pass-thru capability: note that addition by zero must pass the other input, unperturbed, to the output. This corresponds to an additional spatial complexity equal to the total number of non-zero input channels. This is the term linear in k_i.

(2) Additional "U/L" 2x2 LUT: the LUT is appended to identify each input as being upper or lower half of the the range. The table has three output channels: U for both inputs U, L for both inputs L, and B for one input of each. This corresponds to a constant spatial complexity of 4.

(3) "Feedback LUT:" can be realized as a decoder, to detect all possible 3*(m-1) output states, cascaded with an encoder, to transmit the correct output based on the "feedback" rules for addition. This most general case corresponds to the spatial complexity term linear in m (3m-3 for the decoder) with element dynamic range of p+1:1 required.

Note that with the "direct" approach, the data format is different for addition than for multiplication, requiring an additional re-encoding stage between any pairs of successive additions and multiplications. This result is best seen when the MAU is constructed. Westinghouse has introduced the "logarithmic" method for addition (based on the logarithmic transformation we discussed earlier), which provides for common data representation in both LUTs. This eliminates the need for a re-encoding stage. However, the addition algorithm introduces three sequential operations.

TABLE: COMPONENT COMPLEXITY

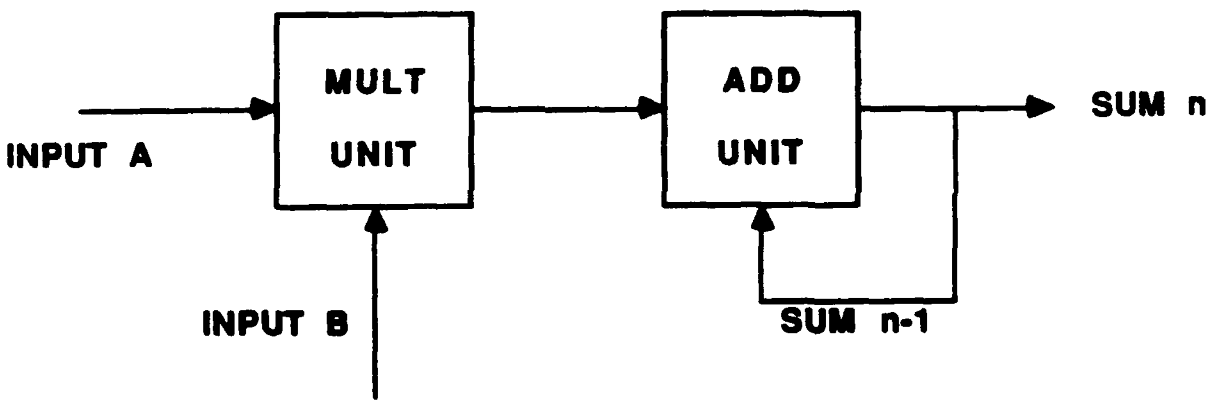
COMPONENT	C_T	C_B	$C_I : C_{PI}, C_{PO}$	C_E
TRANSFORM	0	0	1-1SV	0
ENCODER	0	0	$(m-1)/k_i, p$	$\sim C_{PI}$
DECODER	1	# OP	$p, (m-1)/k_i$	p:1
Z. DETECT	1	1	2	1:0
m^2 LUT	1	m^2	mSV, mSI	2:1
B-ADD	1	$2m-1$	A-D	A-D
B-MULT	1	$2m-2$	A-D	A-D
W-MULT	1	$\sum k_i^2+1$	k_i SV, k_i SI	2:1
W-ADD	2	$\sum k_i^2 + \sum k_i + 3m+1$	k_i SV*, k_i SI*	2:1, p+1:1

DEFINING THE COMPUTATIONAL UNIT

THE MULTIPLY-ACCUMULATE UNIT

* THE MAU PERFORMS THE "SUM OF PRODUCTS" (SOP) OPERATION WHICH IS FUNDAMENTAL IN NUMERICAL COMPUTATION

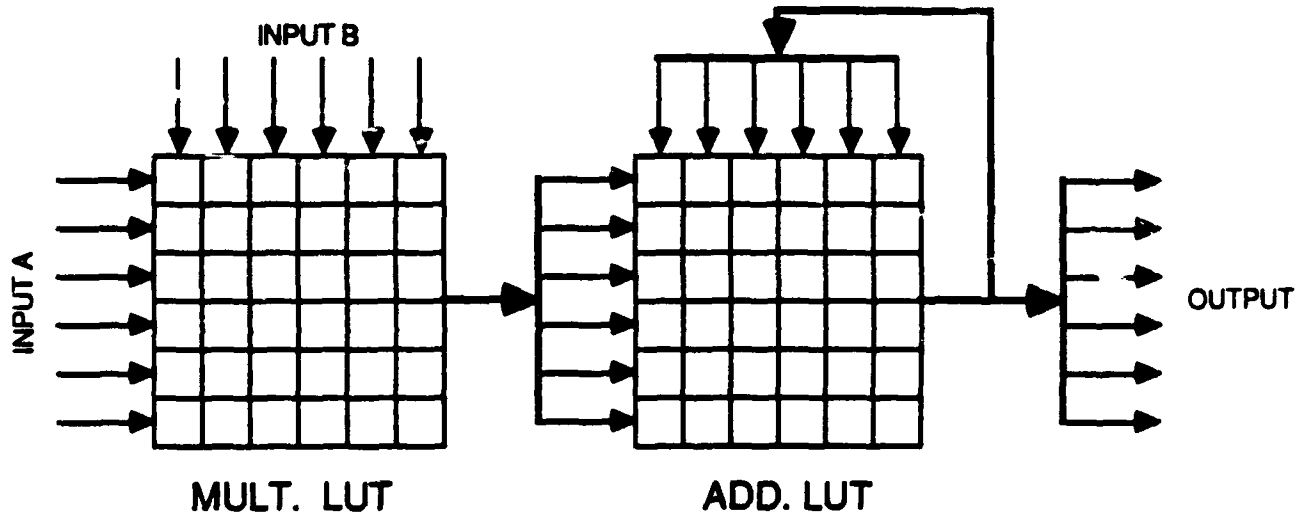
$$|C(i+1)|_m = [\ |A(i)|_m * |B(i)|_m\ ] + |C(i)|_m$$



NOW, WE WILL SPECIFY:

- DIRECT m^2 MAU
- BOEING MAU
- WESTINGHOUSE FACTORED MAU

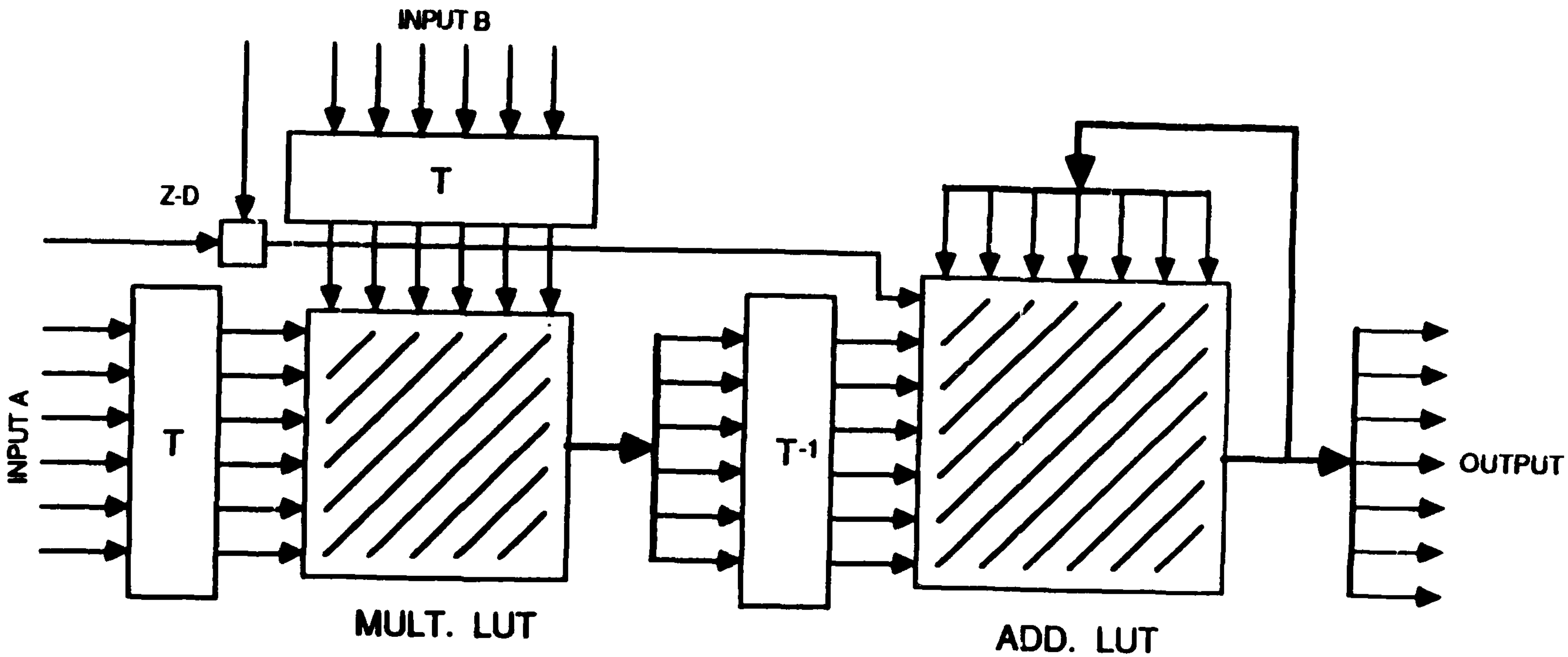
DIRECT m^2 MAU



$$C_T = 2$$

$$C_s = 2m^2$$

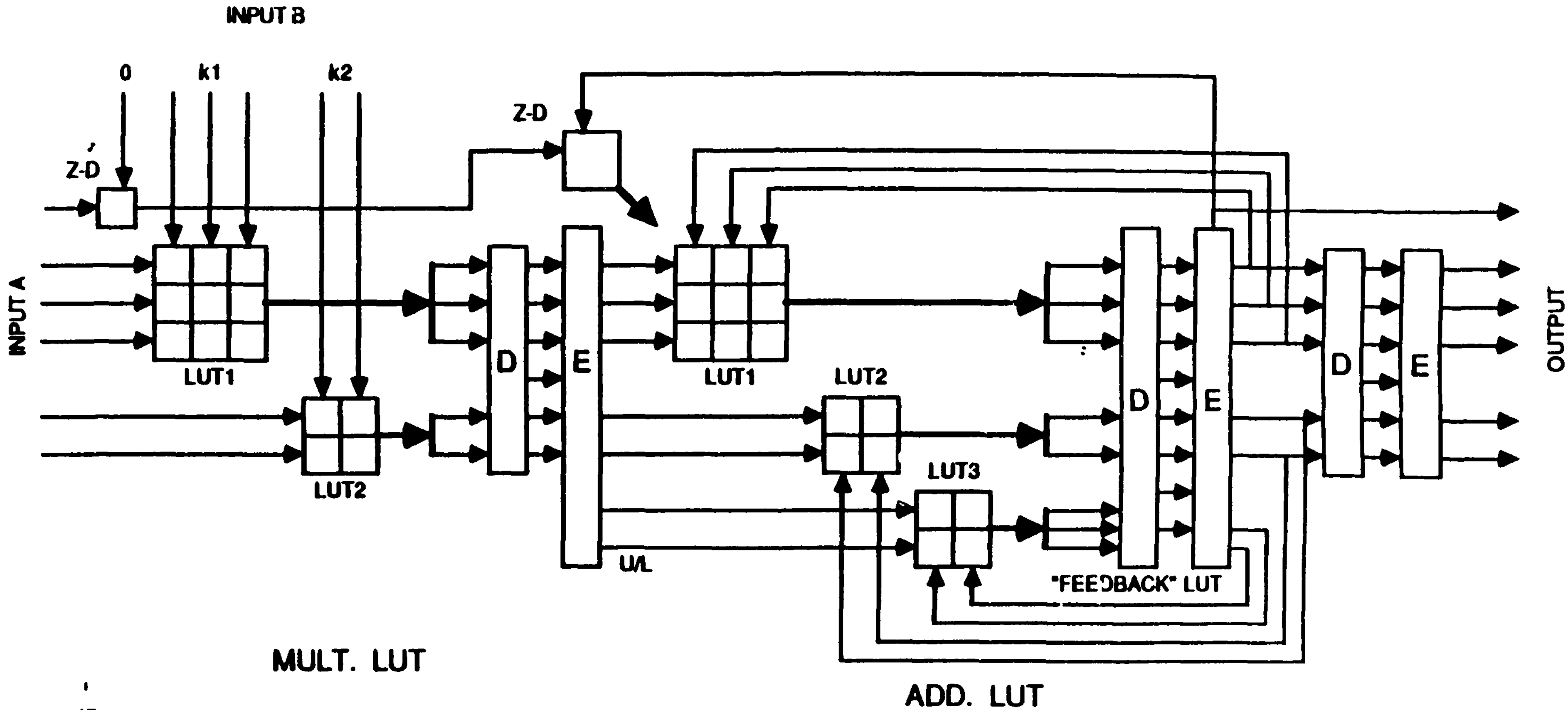
BOEING MAU



$C_T = 2$

$C_B = 4m - 3$

WESTINGHOUSE MAU



$$C_T = 5$$

$$C_B = 2 * \sum_{i=1}^{\rho} k^2 + 2 * \sum_{i=1}^{\rho} k + 5m$$

PERFORMANCE ANALYSIS RESULTS:

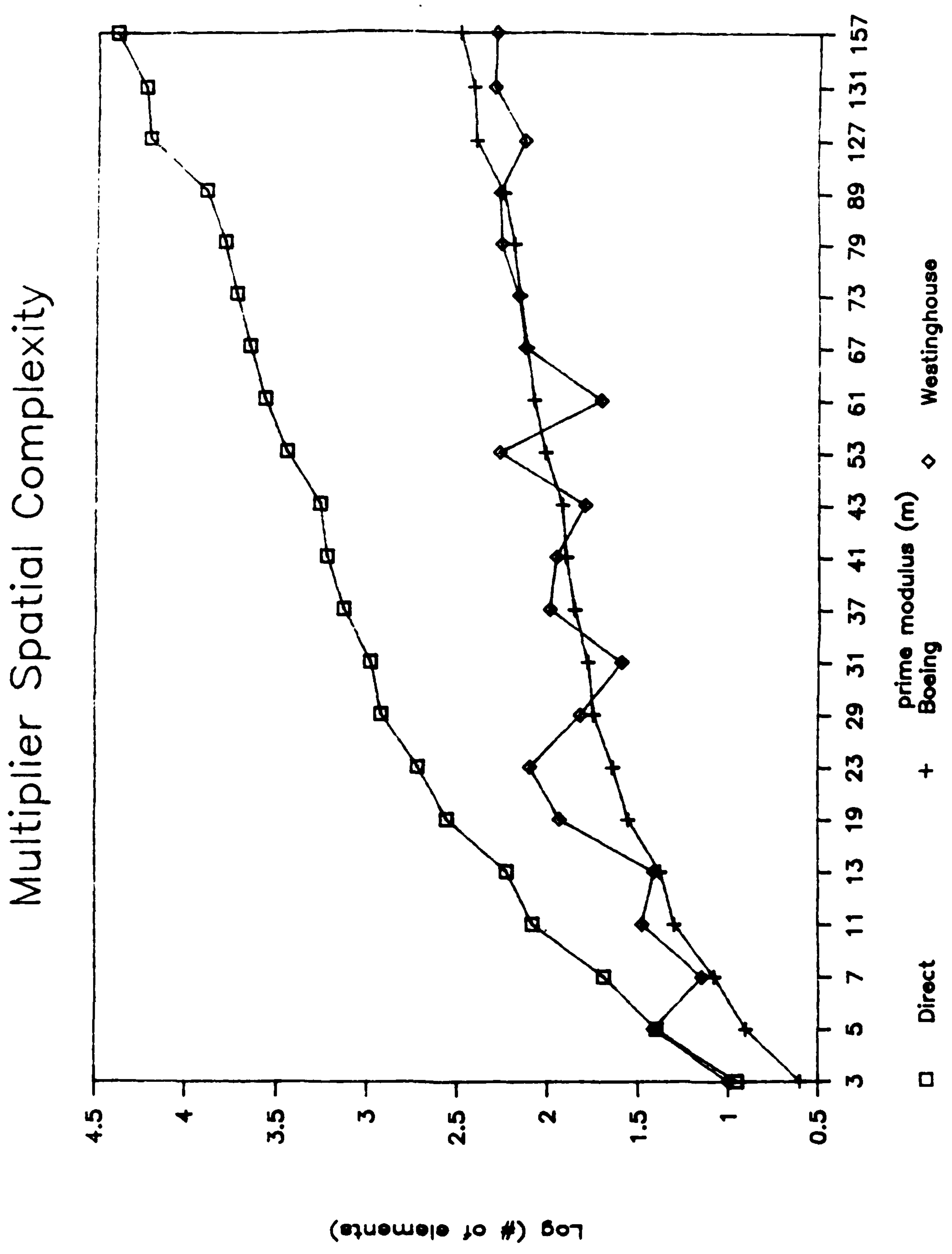
THE COMPLEXITY OF RNS LUT PROCESSORS

RESULTS

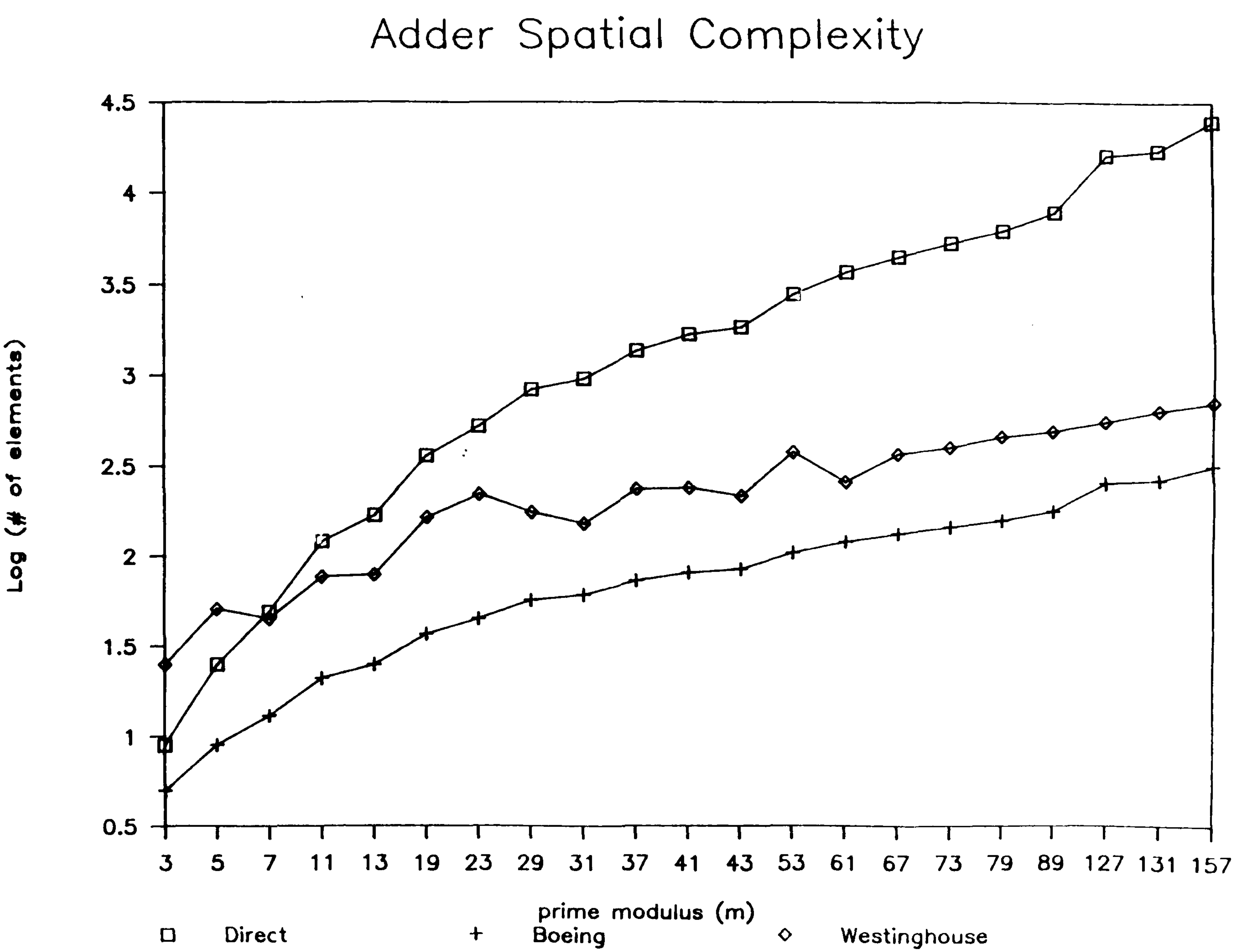
TABLE: COMPLEXITY OF PROCESSING UNITS

UNIT	TEMPORAL COMPLEXITY	ELEMENT COMPLEXITY
MULTIPLIER		
DIRECT	1	2:1
BOEING	1	ARCH.-DEPENDENT
WESTINGHOUSE	1	2:1
ADDER		
DIRECT	1	2:1
BOEING	1	ARCH.-DEPENDENT
WESTINGHOUSE	2	2:1, p+1:1
MAU		
DIRECT	2	2:1
BOEING	2	ARCH.-DEPENDENT
WESTINGHOUSE	5	2:1, p:1, p+1:1

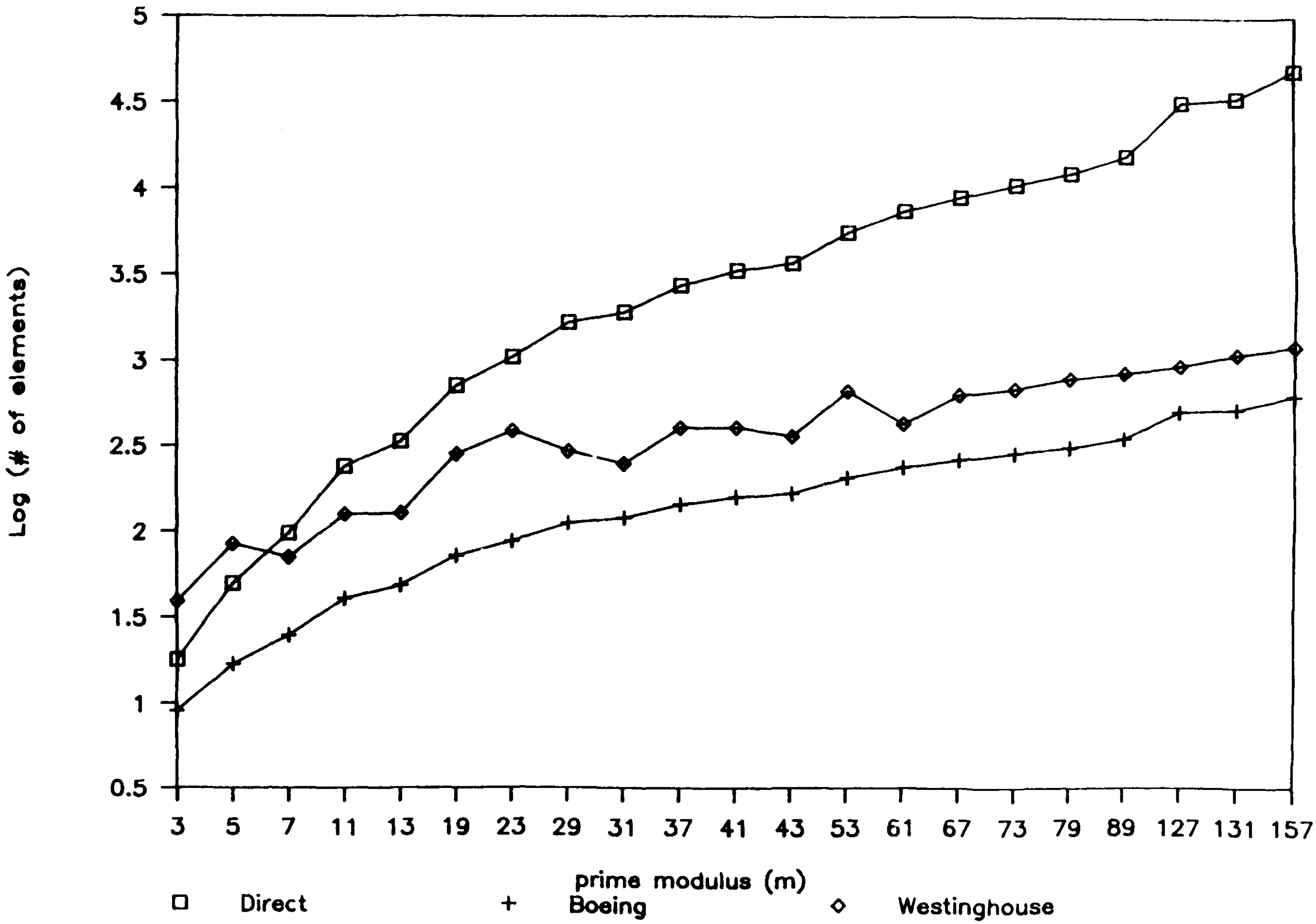
* THE SPATIAL COMPLEXITY SHOWS A STRONG DEPENDENCE ON MODULI, WHICH IS BEST SEEN IN GRAPHICAL FORMAT



Multiplier Spatial Complexity
Log (# of elements)
4.5
4
3.5
3
2.5
2
1.5
1
0.5
3 5 7 11 13 19 23 29 31 37 41 43 53 61 67 73 79 89 127 131 157
prime modulus (m)
Direct
Boeing
Westinghouse


Adder Spatial Complexity
4.5
4
3.5
3
2.5
2
1.5
1
0.5
Log (# of elements)
3
5
7
11
13
19
23
29
31
37
41
43
53
61
67
73
79
89
127
131
157
prime modulus (m)
Direct
Boeing
Westinghouse

MAU Spatial Complexity



NOTES ON SPATIAL COMPLEXITY RESULTS

- The modulus axis is not linear.
- The moduli were chosen based upon those listed for factoring by Goutzoulis (LA-SPIE, 1988).
- The Complexity axis is a Log_{10} scale.

MULTIPLIER SPATIAL COMPLEXITY

- The upper bound is quadratic in m (m^2).
- The Boeing plot is linear in m (2m-2).
- The Westinghouse plot is heavily-dependent upon the factorization.
- At m=157, both approaches exhibit approx. two orders of magnitude reduction in complexity over the Direct.
- As m increases, the oscillation of the West. plot dampens.
- Relative magnitudes:
  - m=23 -> factor of 3 between Boeing and West.
  - m=61 -> factor of 2.5 between West. and Boeing
  - m=157 -> factor of 1.5 between West. and Boeing

ADDER SPATIAL COMPLEXITY

- Upper bound and lower bound are quadratic and linear complexities, respectively.
- Linear term in West. complexity dominates.
- Boeing complexity remains the same.
- At m=157, both approaches demonstrate reductions in complexity of at least 35 over the Direct.
- Relative magnitudes:
  - m=23 -> factor of 5 between Boeing and West.
  - m=61 -> factor of 2 between Boeing and West.
  - m=157 -> factor of 2 between Boeing and West.

MAU SPATIAL COMPLEXITY

- Upper bound and lower bound are quadratic ($2m^2$) and linear (4m) complexities, respectively.
- Results almost identical to adder results
- Linear terms in West adder dominate.
- At m=157, both approaches demonstrate reductions in complexity of at least 35 over the Direct.
- Relative magnitudes:
  - m=23 -> factor of 4 between Boeing and West.
  - m=61 -> factor of 2 between Boeing and West.
  - m=157 -> factor of 2 between Boeing and West.

CONCLUSIONS

* THE SECOND LEVEL FACTORING AND THE USE OF CYCLIC PROPERTIES BOTH LEAD TO LINEAR SPATIAL COMPLEXITY LOOK-UP TABLE PROCESSORS.

* THE TIME COMPLEXITY IS INDEPENDENT OF MODULUS SIZE

* THE ELEMENT COMPLEXITY (DYNAMIC RANGE) SHOWS A MODERATE DEPENDENCE ON MODULI

* GLOBAL, SPACE-VARIANT INTERCONNECTS WITH MODERATE (10-100) FAN-IN AND FAN-OUT REQUIRED

HARDWARE CONSIDERATIONS:

A SUMMARY

HARDWARE CONSIDERATIONS

* THE RNS OPTICAL COMPUTING UNITS CONSISTS OF:
  - INTERCONNECTS (BETWEEN UNITS AND WITHIN UNITS)
  - ACTIVE SWITCHING ELEMENTS (LUTs AND DECODERS)

* THERE ARE A NUMBER OF CHOICES FOR EACH OF THE CONSTITUENTS. THE HARDWARE SELECTION FOR EACH CONSTITUENT WILL BE GUIDED BY THE ALGORITHM AND ARCHITECTURE

* THE SYSTEM PERFORMANCE (COMPUTATIONAL THROUGHPUT, POWER CONSUMPTION, SPATIAL COMPLEXITY, INTERFACE REQUIREMENTS, MECHANICAL STABILITY) IS DETERMINED BY COMBINING THE HARDWARE CHARACTERISTICS WITH THE ALGORITHM / ARCHITECTURE CHARACTERISTICS

INTERCONNECTS

USES:

* BETWEEN COMPUTING UNIT (1-1)
* ENCODERS (1-M, IRREGULAR, 1-D)
* DECODERS (M-M, IRREGULAR, 1-D)
* LOOK UP TABLES (1-M, REGULAR, PLANAR FOR INPUTS; M-1, IRREGULAR, 3-D FOR OUTPUTS; M-1, REGULAR, PLANAR FOR OUTPUTS IN SYMMETRIC)

TECHNOLOGIES

* FIBER OPTIC INTERCONNECTS ARE FLEXIBLE, RUGGED, 3-D, EFFICIENT AND EASY TO DEMONSTRATE
  - DON'T SCALE WELL
  - DIFFICULT TO AUTOMATE

* INTEGRATED OPTICAL INTERCONNECTS ARE FLEXIBLE, RUGGED, EFFICIENT, WILL SCALE WELL AND EASILY AUTOMATED
  - INHERENTLY PLANAR (NOT SUITED TO LUTs)

* FREE-SPACE OPTICAL INTERCONNECTS ARE FLEXIBLE, SCALE WELL AND EASILY AUTOMATED
  - TIGHT ALIGNMENT TOLERENCES
  - INEFFICIENT

* FOURIER OPTICAL INTERCONNECTS HAVE SPECIAL SYMMETRIES
  - COHERENT ILLUMINATION REQUIRED

ACTIVE SWITCHING ELEMENTS

USES

* DECODERS (P-INPUT AND GATES)
* LOOK UP TABLES (2-INPUT AND GATES, m-INPUT WIRED OR GATES- ENTAILS SPATIAL COMPLEXITY)

TECHNOLOGIES

* ALL-OPTICAL NONLINEAR DEVICES
  - HIGH SPEED, COMPATIBLE INPUT / OUTPUT, 2-D PARALLEL OUTPUT, LOW FAN-IN / OUT, CONTRAST
  - HIGH POWER CONSUMPTION, IMMATURE TECHNOLOGY

* HYBRID TECHNOLOGIES
  - LASER DIODE ARRAYS
    - HIGH SPEED, LARGE POWER CONSUMPTION
  - GUIDED WAVE OPTICAL SWITCHES
    - HIGH SPEED, LARGE POWER CONSUMPTION, 1-D ARRAYS
  - SPECIAL PURPOSE DEVICES (1-D ACOUSTOOPTIC POINT MODULATOR ARRAYS, MAGNETOOPTIC LIGHT MODULATOR)
    - IMMATURE TECHNOLOGIES, POWER-SPEED LIMITS NOT WELL ESTABLISHED

INTERACTION BETWEEN ARCHITECTURES AND HARDWARE

* BOEING APPROACH OF UTILIZING LINEAR COMPLEXITY IS BASED ON FOURIER OPTICS FOR SHIFT-INVARIANT INTERCONNECTS.

* ARCHITECTURE AMENABLE TO INTEGRATED OPTICAL IMPLEMENTATION WITH HIGH SPEED MODULATORS

* THE LARGE AREA DETECTOR REQUIRED IN THE OUTPUT MAY POSE THE PRIMARY LIMIT ON THE SPEED OF THE SYSTEM

* IF THE DETECTOR AREA CAN BE REDUCED, THE OVERALL SYSTEM EFFICIENCY COULD CHANGE

SUMMARY

* RESIDUE NUMBER SYSTEM CAN BE EFFECTIVELY USED APPLICATIONS WITH LARGE NUMBER OF MULTIPLY-ADD/SUBTRACT AND VERY FEW DIVISIONS, COMPARISONS, SIGN DETECTION

* POSITION CODED RESIDUE REPRESENTATION LEADS TO EFFECTIVE LOOK UP TABLE COMPUTING

* SWITCHING REQUIREMENTS OF LUTs ARE MODEST IN TERMS OF FAN-IN / OUT AND CONTRAST

* SPATIAL COMPLEXITY AND SWITCHING ELEMENT COMPLEXITY DEPEND VERY STRONGLY ON THE ALGORITHM AND THE MODULUS

* IMPACT OF DIFFERENT DEVICE TECHNOLOGIES ON ALGOTECTURE PERFORMANCE MERITS FURTHER STUDY

* DELINIATION OF DOMAINS OF APPLICABILITY OF RESIDUE NUMBER SYSTEM MERITS FURTHER STUDY

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